

polysilicon; (4) deposited one second polysilicon on the activated and doped first polysilicon; (5) doping the second polysilicon; (6) activating the doped second polysilicon; (7) with phosphorus acid, etching the activated and doped second polysilicon, forming one bottom plate consisting of polysilicon with rugged surface.

Dwg.0/7

*look draw  
then draw the next*

L48 ANSWER 6 OF 8 WPIX (C) 2003 THOMSON DERWENT

AN 1996-392014 [39] WPIX

DNN N1996-330380 DNC C1996-123314

TI Fabrication method of stack DRAM with rugged surface - using rugged surface as storage node of capacitor to increase capacitance.

DC L03 U11 U13 U14

IN IAN, H; LIAW, J

PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP

CYC 1

PI TW 278239 A 19960611 (199639)\* 17p

ADT TW 278239 A TW 1995-106348 19950620

PRAI TW-1995-106348 19950620

AB TW 278239 A UPAB: 19961004

A fabrication method of stack DRAM with rugged surface comprises: (a) forming field effect transistor in silicon semiconductor substrate, in which the field effect transistor includes gate oxide, gate electrode and source/drain electrode regions; (b) forming transistor node contact of stack dynamic random access memory; (c) removing native oxide of the above transistor source surface; (d) forming one undoped second polysilicon layer; (e) removing native oxide of the above undoped second polysilicon layer surface; (f) forming on in-situ doped third polysilicon; (g) removing native oxide of the above in-situ doped third polysilicon layer surface; (h) depositing one amorphous silicon in high vacuum environment, and raising temp. in original high vacuum environment, performing post anneal process to the above amorphous silicon by N gas with high purity, so as to convert the above amorphous silicon to rugged-surface polycrystalline silicon; (i) removing native SiO<sub>2</sub> layer of node contact surface; (j) by plasma etching defining the pattern of undoped second polysilicon, in-situ third polysilicon and rugged surface polycrystalline silicon to form capacitor storage node; (k) forming one capacitor dielectric on the above storage node; (l) forming one doped fourth polysilicon on the above capacitor dielectric; and (m) by plasma etching defining the pattern of the above doped fourth polysilicon as top electrode of stack capacitor.

Dwg.9/9

L48 ANSWER 7 OF 8 WPIX (C) 2003 THOMSON DERWENT

AN 1989-090625 [12] WPIX

TI Memory capacitor for semiconductor dynamic RAM - has impurity-doped poly silicon capacitor electrode with rugged surface NoAbstract Dwg 1/4.

DC U12

PA (HITA) HITACHI LTD

CYC 1

PI JP 01042161 A 19890214 (198912)\* 3p

ADT JP 01042161 A JP 1987-198043 19870810

PRAI JP 1987-198043 19870810

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